CS/IS46

USN

NEW SCHEME

Fourth Semester B.E. Degree Examination, July 2006
EC/TE/EE/IT/ML/BM/CS/IS
Computer Organization

Time: 3 hrs.] [Max. Marks:100

Note: *1. Answer any FIVE full questions.*
2. Answer should be brief and to the point.

1 a. Distinguish between :
i) Pipelining and super scalar operation
ii) CISC and RISC
iii) Multiprocessors and multicomputers. (09 Marks)
b. Explain clearly SPEC Rating and its significance. (03 Marks)
c. Convert the following pairs of numbers to 5 bit signed 2's complement binary numbers and add them. State whether an overflow occurs in each case.
i) -14 and 11 ii) -10 and -13. (04 Marks)
d. Discuss the two ways in which byte addresses are assigned across words. (04 Marks)

2 a. Explain with a specific example how a stack frame is built and dismantled for a particular invocation of a subroutine. (08 Marks)
b. Which of the following possibilities for saving return address of a subroutine support subroutine nesting and which support subroutine recursion and why?
i) in a processor register ii) in a memory location associated with call
iii) on a stack. (04 Marks)
c. Explain clearly the Bus Arbitration Methods. (08 Marks)

3 a. Draw a combined input / output interface circuit and explain the different operations clearly. (10 Marks)
b. Consider a synchronous bus that transfers data in one clock cycle. Address transmitted by the processor appears on the bus after 4 nanoseconds, propagation delay on the bus varies from 1 to 5 nanoseconds, address decoding takes 6 nanoseconds. Addressed device takes 5 to 10 nanoseconds to place the data on the bus. Input buffer needs 3 nanoseconds setup time. Estimate the clock speed at which this bus can operate. (04 Marks)
c. Distinguish between the processor clock speed and bus clock speed and explain why the disparity occurs between the two. State the values of the above in a modern computing system. (06 Marks)

4 a. Discuss the main phases involved in the operation of SCSI bus in detail. (10 Marks)
b. Explain the operation of a split bus with a diagram. (05 Marks)
c. With a diagram explain USB packet format clearly. (05 Marks)

5 a. Draw a block diagram for 8m X 32 memory system using 512 k X 8 memory chips and explain its operation. **(08 Marks)**

b. Discuss direct mapped, associative mapped and set associative mapped CACHE memory system with suitable diagrams. **(08 Marks)**

c. Define Hit Rate and Miss Penalty. **(04 Marks)**

6 a. Show the organization of a typical associative mapped TLB and explain how address truncation takes place. **(10 Marks)**

b. Explain the organization and how data is accessed from a disk. State the typical values for recording surfaces, tracks, sectors, bytes / sectors, access time in a disk. **(10 Marks)**

7 a. Discuss the Booth's Multiplication Algorithm with an example. **(10 Marks)**

b. With a clear diagram explain the floating point addition – subtraction unit. **(10 Marks)**

8 a. With a diagram which shows the separation Decoding and Encoding functions. Explain hard wired control **(10 Marks)**

b. With a block diagram explain an embedded processor with all the salient blocks and their functions. **(10 Marks)**

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